REMARKS

Claims 1-11, 13-15, and 17-29 are all the claims presently pending in the application. Claims 1, 4, 6, 9, 11, 17, and 23 are amended to more clearly define the invention and claims 12 and 16 are canceled. Claims 1, 6, and 11 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Support for these amendments may be found in the specification at, for example, page 9, lines 14 - 23 and page 10, lines 12-22).

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements.

Claims 1-11 and 14-26 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Green, et al. (U.S. Patent No. 5,773,341). Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Green. Claims 27-29 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Green in view of Toyokawa, et al. (U.S. Patent No. 6,576,509).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

An exemplary embodiment of the claimed invention, as defined by, for example, independent claim 11, is directed to a method for fabricating a semiconductor device. The method includes depositing a metallic conductive film on an underlying insulating film, depositing a first insulator film on the metallic conductive film, depositing a second insulator

film on the first insulator film, patterning the first and second insulator films, etching the second insulator film to have a patterned area that is smaller than the first insulator film, and patterning the metallic conductive film, and subsequently depositing a third insulator film on the first insulator film, said etched second insulator film, and the insulating film.

Conventional methods for fabricating semiconductor devices have problems with defects such as a void and/or a short-circuit.

For example, in a first conventional method a two-layer mask is used to pattern a bit line. However, the use of a two-layer mask tends to increase the depth of sidewall films and, therefore, increases the aspect ratio between the depth of the sidewall films and the space between the sidewall films. This increased aspect ratio increases the likelihood that a defect, such as a void, is formed in an interlayer dielectric film. (Page 3, line 2 - 10).

In a second conventional method, a single-layer mask may be used to pattern a bit line. The use of a single-layer mask provides a reduced thickness in comparison to a two-layer mask and generally reduces the likelihood of forming a defect, such as a void, in an interlayer dielectric film. However, this reduction in thickness may result in an exposure of the bit lines when a contact hole is formed. This may result in a short-circuit defect. (Page 4, lines 3-23).

In summary, a two-layer hard mask may cause a defect in the embedding structure due to the increased aspect ratio, while a single-layer hard mask may cause a short circuit failure. (Page 5, lines 2-10).

In stark contrast, the present invention solves these problems by etching the second insulator film to have a patterned area that is smaller than the first insulator film. In this manner, the present invention reduces the likelihood of a short circuit failure while enabling

the use of a two-layer mask. (Page 6, lines 1 - 6).

Further, in accordance with an exemplary embodiment of the claimed invention the third insulating layer is deposited subsequently to the etching of the second insulator film because the shape of the etched second insulator film affects the shape of the deposited third insulating layer. In this manner, the shape of the tapered mesa structure can be adjusted by adjusting the etching of the second insulator film. (Page 9, lines 14 - 23).

II. THE 35 U.S.C. § 112, SECOND PARAGRAPH REJECTION

The Examiner alleges that claim 23 is indefinite. While Applicant submits that such would be clear to one of ordinary skill in the art to allow them to know the metes and bounds of the invention, taking the present Application as a whole, to speed prosecution claim 23 has been amended in accordance with Examiner Novacek's very helpful suggestions.

In view of the foregoing, the Examiner is respectfully requested to withdraw this rejection.

III. THE PRIOR ART REJECTIONS

A. The Green et al. reference

Regarding the rejections of claims 1-26, the Examiner alleges that the Green et al. reference teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by the Green et al. reference.

None of the applied references teaches or suggests the features of the claimed invention including a method for fabricating a semiconductor device that etches the second insulator film to have a patterned area that is smaller than the first insulator film and that

subsequently deposits a third insulator film on the first insulator film, the etched second insulator film, and the insulating film. As explained above, these features are important for reducing the likelihood of a short circuit failure while enabling the use of a two-layer mask and for controlling the shape of the tapered mesa structure.

In stark contrast, the Green et al. reference discloses depositing the third insulator film (sidewall spacers 45 and 46) before etching of the second insulator film (second capping layer 26). Indeed, the Green et al. reference explains that etching of the second capping layer 26 after the sidewall spacers 45 and 46 are deposited results in the forming of recesses 48b and 50b by masking "some of said material between the respective pairs of sidewall spacers" (col. 4, lines 31-34) "thus providing a gap between the respective inner sidewall spacers" (emphasis added, col. 4, lines 56-57).

Clearly, the Green et al. reference does not teach or suggest a method for fabricating a semiconductor device that etches the second insulator film to have a patterned area that is smaller than the first insulator film and that subsequently deposits a third insulator film on the first insulator film, the etched second insulator film, and the insulating film.

Applicant respectfully requests withdrawal of the rejections of claims 1-26.

B. The Green et al. reference in view of the Toyokawa et al. reference

Regarding the rejection of claims 27-29, the Examiner alleges that the Toyokawa et al. reference would have been combined with the Green et al. reference to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

None of the applied references teaches or suggests the features of the claimed invention including a method for fabricating a semiconductor device that etches the second insulator film to have a patterned area that is smaller than the first insulator film and that subsequently deposits a third insulator film on the first insulator film, the etched second insulator film, and the insulating film. These features are important for reducing the likelihood of a short circuit failure while enabling the use of a two-layer mask and for controlling the shape of the tapered mesa structure.

As explained above, the Green et al. reference does not teach or suggest these features.

The Toyokawa et al. reference does not remedy the deficiencies of the Green et al. reference.

Rather, the Toyokawa et al. reference merely discloses another semiconductor integrated circuit device having a dynamic random access memory. The Toyokawa et al. reference does not teach or suggest anything at all about providing a second insulating film, let alone etching the second insulator film to have a patterned area that is smaller than the first insulator film and subsequently depositing a third insulator film on the first insulator film, the etched second insulator film, and the insulating film.

Indeed, the Examiner does not allege that the Toyokawa et al. reference teaches or suggests these features.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 27-29.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-11, 13-15, and 17-29, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 1/12/06

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